REMARKS

This paper is being provided in response to the June 4, 2002 Final Office Action for the above-referenced application. In this response, applicant has amended claims 1 and 6 in order to clarify Applicant's claimed invention. Applicant respectfully submits that the amendments to the claims are supported by the originally filed specification.

In response to the objection to claims 1 and 6, applicant has amended claims 1 and 6 to clarify that the first drain and source layers are diffusion layers. Accordingly, applicant respectfully requests that this objection be withdrawn.

The rejection of claims 1-11 and 20-23 under 35 U.S.C. 112, first paragraph, as containing subject mater not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor had possession of the claimed invention, is hereby traversed. The Office Action suggests that figure 4 does not show that the first S/D diffusions surrounding the second diffusions on at least a bottom and four lateral sides, since the fourth edge of both first and second diffusions abut the STI region 2. Applicant respectfully disagrees and notes that the first diffusions 63 and 64 abut the STI region 2 at a lower position, which is therefore more laterally displaced due to the slope of the STI region, as shown in the figures.

The Office Action further suggests that there is no support for two first diffusions and only one side wall offset extending along a lateral surface of a gate oxide film, as

recited in claims 20 and 22. Applicant respectfully disagrees and notes that the prior art figures 1 and 2 show the presence of lightly doped regions under the thin gate oxides 152 and 252 and thus represent two first S/D diffusions in conjunction with the second diffusions 165 and 166, even though in the prior art there are no sidewall offsets. Further, figure 4 does show that there is a sidewall 53 that does not have an offset region 54a, and thus there will be two first S/D diffusions, even though there is only one sidewall offset, since there still are two sidewalls. Accordingly, applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 1-11 and 20-23 under 35 U.S.C. 112, second paragraph, as being indefinite, has been addressed by the claims amendments contained herein. In particular, the claims amendments now clarify that the lateral surface of said sidewall is the vertical thickness in question. Accordingly, applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 1, 3-6, 9-11, 20 and 22 under 35 U.S.C. 103(a) as being obvious over Gonzales (U.S. Patent No. 5,439,835, hereinafter referred to as "Gonzales") in view of Cheng (U.S. Patent No. 5,545,575, hereinafter referred to as "Cheng") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims 1, 3-6, 9-11, 20 and 22, as amended herein, are neither disclosed nor suggested by the suggested combination of references.

Applicant's claim 1, as amended herein, recites a semiconductor device with a gate electrode and first drain and source diffusion layers formed around the gate electrode and at least one sidewall that extends laterally. There are second drain and source diffusion layers surrounding the first drain and source electrodes and aligned to the sidewall. The sidewall has a horizontal offset extending by more than the vertical thickness of the lateral portion of the sidewall. At least one of the drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset.

Applicant's claim 6, as amended herein, recites a semiconductor device including a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated, and a gate electrode formed on the semiconductor substrate, the gate electrode and the insulating film defining lightly doped first drain and source diffusion layers. There is at least one sidewall covering the gate electrode, and heavily doped second drain and source diffusion layers formed at a surface of the semiconductor substrate around the gate electrode and aligned with the sidewall covering, with the first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides. The sidewall has a sidewall offset extending outwardly of the gate electrode along a horizontal surface of the semiconductor substrate in at least one region below which at least one of the second drain and source diffusion layers are formed. The sidewall offset extends along a lateral surface of the gate oxide film on which the gate electrode is formed by an amount that is greater than the vertical thickness of the lateral surface of the sidewall, and there are low-resistive wiring layers formed at

the surface of the drain and source diffusion layers, located outwardly beyond a peripheral edge of the sidewall and offset in at least one drain and source diffusion layer. At least one of the drain and source diffusion layers extends towards the gate electrode beyond an edge of the sidewall offset.

Dependent claims 3-5, 9-11, 20 and 22 depend from the independent claims, and add further patentable features such as the feature of adding a memory cell, and lowering the diffusion concentration of the drain and source diffusions.

The cited reference of Gonzales discloses a process for fabricating a CMOS DRAM using a high energy ion implantation of boron ions at a oblique angle for punch through protection. The graded junction 24B is formed by the oblique implantation. The junction of the diffusion is not aligned to the edge of the sidewall offset over gates 16 and 17.

The cited reference of Cheng is used in the Office Action to show that first S/D diffusion may surround second S/D diffusions and have different diffusion concentrations. Cheng discloses an insulated gate semiconductor device having gate electrodes, and a source region 57 nested inside source region 43, etc. Openings in a layer of dielectric material 63 expose portions of the S/D regions to form Silicide 64.

The Office Action suggests that the failure of the cited reference of Gonzales to disclose that the diffusion is aligned to the edge of the offset is not important since the

present independent claims do not specifically recite that feature. Applicant respectfully submits that a recitation of a " ... heavily doped second drain and source diffusion layers formed at a surface of said semiconductor substrate *around* said gate electrode and said at least one sidewall covering, ..." would clearly be understood by one of ordinary skill in the art to mean that the diffusion is aligned with the sidewall. In addition, Applicant has added language to the independent claims to further clarify the relationship between the diffusion and the sidewall and sidewall offset.

Further, Gonzales does not even have a sidewall film that has anything what so ever to do with the diffusion, nor does it extend laterally away from the gate by an amount greater than the thickness of the sidewall, as recited in the present independent claims. Gonzales figure 9 especially shows that the drain 24A near isolation region 13 is aligned to the gate electrode 16, and the isolation oxide 13, and not by the unlabeled sidewall film.

Yet further, the present invention has metal lines that are in direct contact with the sidewall film, and this feature is also not found in the cited references, and certainly not Gonzales, which has no silicide films such as found in the present claimed invention.

Applicant further respectfully submits that the cited reference of Cheng does little to correct the above noted deficiencies of the Gonzales reference, such as the failure to have lateral sidewall offsets that are used to align the S/D diffusions. Thus the suggested combination of references, even if properly combinable, still does not disclose or suggest

all of the claimed features. Specifically, the cited references neither describe nor suggests at least the combination of features of a "... *heavily doped second drain and source diffusion layers formed ... around said gate electrode and aligned with said at least one sidewall covering, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and four lateral sides, said at least one sidewall having a sidewall offset extending ... along a horizontal surface of said semiconductor substrate ... said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a vertical thickness of said lateral surface of said sidewall ...*", as recited in independent claims 1 and 6, as amended herein.

Applicant respectfully submits that the cited references do not disclose a sidewall offset that has an extent that is greater than the vertical thickness of the lateral portion of the sidewall, and defines diffusions. Cheng is used by the Office Action to show nested S/D diffusions, but discloses no horizontal portion of the sidewall films 37 and 49, or 38 and 52 etc. That this is required by Cheng is clear since Cheng defines (i.e., aligns) the sidewall location by an anisotrophic timed etch process, and thus can not possibly have a lateral offset such as found in the present claimed invention. Even mislabeling the protection film 66 of Cheng as a sidewall does not align the S/D as recited in Applicant's claims.

The dependent claims are felt to be patentable at least as depending upon a base claim shown above to be patentable. Therefore, applicant respectfully requests that this rejection be withdrawn.

The rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over Gonzales in view of Cheng, and further in view of Kunishima, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claim 7 is neither disclosed nor suggested by the suggested combination of cited references, whether taken separately or in any combination.

Dependent claim 7 recites that the low resistance wiring is formed from TiSi.

The Gonzales and Cheng references are discussed above, as are the features of independent claim 6, from which claim 7 depends.

The cited reference of Kunishima is apparently used by the Office Action to show the missing feature of TiSi. Kunishima generally discloses a FET with SiO2 and BPSG films deposited on a substrate and then lamp annealed to increase the concentration of the p+ type impurity diffusion layer. There is a $TiSi_2$ layer 21 shown in Figure 5C, and discussed at column 10, lines 16-59.

Applicant respectfully submits that the cited reference of Kunishima does not correct the defects of the cited Gonzales and Cheng references discussed above.

Kunishima neither describes nor suggests a sidewall offset extending along a surface of a gate oxide film on which the gate electrode is formed, as set forth in applicant's amended claim 6, from which dependent claim 7 depends. Applicant respectfully submits that dependent claim 7, is patentable at least as depending upon a base claim shown above to be patentable. In view of the foregoing, applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1-4, 6, 8-10, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims 1-4, 6, 8-10, 21 and 23 are neither described nor suggested by the cited reference, whether taken alone, or in any combination with well known art.

Independent claims 1 and 6 have features that are summarized above. Claims 2-4 depend from claim 1. Claims 8-10, 21 and 23 depend from claim 6. The cited reference of Cheng is discussed above.

Applicant respectfully submits that since independent claims 1 and 6 have been shown to be patentable over Cheng in view of Gonzales, then the claims are also patentable over Cheng, whether taken alone, or in any combination with other known references.

Specifically, the suggested reference of Cheng neither describes nor suggests the combination of features of a "*...heavily doped second drain and source diffusion layers formed ... around said gate electrode and aligned with said at least one sidewall covering, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and four lateral sides, said at least one sidewall having a sidewall offset extending ... along a horizontal surface of said semiconductor substrate ... said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a vertical thickness of said lateral surface of said sidewall ...*", as recited in independent claims 1 and 6, as amended herein, as discussed above. Cheng does not suggest that the sidewall extends along the surface to limit the location of the diffusions, and can not do this since there is no masking of the sidewalls, just an anisotrophic etch. Therefore, the suggested feature can not exist in the cited reference, and thus the cited reference is improperly cited in this instance. Therefore the independent claims 1 and 6, as amended herein, and thus the dependent claims based upon them, are non obvious over Cheng, since Cheng can not form the offset portion of the sidewall. In view of the foregoing, applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 5, 7, 11, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Kunishima, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims 5, 7, 11, 21 and 23 are neither disclosed nor suggested by the suggested combination of cited references, whether taken alone, or in any combination.

The Cheng and Kunishima references are discussed above. The features of the independent claims upon which dependent claims 5, 7, 11, 21 and 23 are based are also discussed above. The Office Action uses Kunishima to shows the missing feature of TiSi.

Applicant respectfully submits that the addition of a silicide layer to Cheng still does not provide Cheng with any disclosure with regard to a "*...heavily doped second drain and source diffusion layers formed ... around said gate electrode and aligned with said at least one sidewall covering, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and four lateral sides, said at least one sidewall having a sidewall offset extending ... along a horizontal surface of said semiconductor substrate ... said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a vertical thickness of said lateral surface of said sidewall* ...", as recited in independent claims 1 and 6, as amended herein, as previously discussed above. Thus Cheng, which was shown above to not render the independent claims obvious, still does not render the independent claims obvious, and thus the dependent claims are patentable.

In view of the above discussion, applicant respectfully requests that this rejection, as set forth in the Office Action, be reconsidered and withdrawn.

Applicant respectfully submits that the Cheng reference does not disclose a sidewall offset that aligns the diffusions that is displaced by more than the thickness of the horizontal portion of the sidewall offset. Figure 15 of Cheng does not, as suggested in the Office Action, teach a sidewall offset that extends along a lateral surface of a gate oxide by an amount that is greater than a vertical thickness of the sidewall. The oxide 66 of Cheng is not a sidewall film at all, as would be clear to one of ordinary skill in the art, since it is not used to define or align the diffusions 57 or 43, etc., which are defined by the polysilicon, and the supposed sidewall is used to form the silicide regions 64, rather than the diffusions. Likewise, figure 9 of Gonzales does not have the unlabeled supposed sidewall film defining the location of the diffusions 24A and 24B, as suggested in the Office Action. Thus the cited references do not teach a "sidewall film", as this term would be understood by anyone of ordinary skill in the art, and as recited in the independent claims, as amended herein to make it clear that the sidewall films are used to align part of the diffusions.

Based on the above, applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
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Date

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